REMARKS

Claims 1-20 are pending in the application.

Claims 1-20 are rejected.

Claims 1-20 are rejected under 35 U.S.C. 102(e).

Claims 1 and 8 are currently amended.

Interview Summary

Applicants thank the Examiner for the telephone interview that was conducted between the Examiner and Applicant's representative, Brian Wichner, on May 12, 2005. During that interview, Applicant's representative argued that Okayasu does not teach or disclose, among other things, multiple pins for each comparator/driver circuit. In particular, Okayasu's relay matrix (105) does not switch single comparator/driver circuits among multiple DUT pins, but instead only switches paths between a DC test unit (116) and the pin P. The Examiner indicated that he agreed with this assessment of Okayasu, but that he believes the claims are very broad and other art could most likely be found to anticipate the claimed invention, even without Okayasu.

Claim Rejections – 35 U.S.C. § 102

Claims 1-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Okayasu (U.S. Patent No. 6,157,200).

Applicants respectfully traverse the rejections.

Claim 1 has been amended to recite that a driver is configured to drive an input signal to be applied to two or more input pins of a semiconductor device, and a comparator is configured to compare data output from two or more output pins of the semiconductor device. No new matter is added. Support may be found in several places in the Specification, including FIG. 2.

Okayasu, however, teaches only a single input/output pin P of a semiconductor device (IC in performance board 101, or DUT) interfaced with each comparator/driver circuit (102A), not multiple pins for each comparator/driver circuit, as in claim 1. Applicants respectfully disagree with the Examiner's opinion that a relay matrix (105) switches the device groups to respective terminals of the DUT. On the contrary, the relay matrix (105) is only used to switch paths between a DC test unit (116) and the pin P. "During the DC test, the pin electronics (102A) is disconnected from the pin P of the DUT but instead the DC unit

(116) is connected thereto (col. 5, lines 58-67). Furthermore, Okayasu teaches the pin electronics (102A) with a driver (103A) for driving *one* terminal P of the DUT (col. 5, lines 15-16). Again, the applicants respectfully disagree with the Examiner's opinion that the pin electronics (102) comprises a plurality of terminals P, each corresponding to respective terminals of the DUT. Applicants assert that this cannot be the case because Okayasu does not show any means for multiplexing a plurality of terminals P with each comparator/driver of the pin electronics (102). Again, the relay matrix (105) is not used for this purpose, but it is only use for switching between the DC test unit (116) and the pin P.

Therefore, it is submitted that claim 1 is patentably distinguishable over the prior art and allowance of this claim is requested.

Claims 2-7 depend from claim 1 and inherently include all of the limitations of the base claim. As discussed above, the prior art does not teach the limitations of the base claim much less the further embodiments of the dependent claims. Therefore, claims 2-7 are allowable for their dependency and their own merits. Allowance of these claims is requested.

Claim 8, amended to recite a single pin, is also not anticipated by Okayasu for at least the reasons explained above. Also, claims 9-11 depend from claim 8 and inherently include all of the limitations of the base claim. As discussed above, the prior art does not teach the limitations of the base claim much less the further embodiments of the dependent claims. Therefore, claims 9-11 are allowable for their dependency and their own merits. Allowance of these claims is requested.

Claim 16 recites a method of testing a semiconductor device having many pins using a test system with fewer pins. Claim 16 is also not anticipated by Okayasu for at least the reasons explained above. Also, claims 17-20 depend from claim 16 and inherently include all of the limitations of the base claim. As discussed above, the prior art does not teach the limitations of the base claim much less the further embodiments of the dependent claims. Therefore, claims 17-20 are allowable for their dependency and their own merits. Allowance of these claims is requested.

Claim 12 recites an input and output pattern memory. The input pattern memory (62) is defined in the Specification, page 8, line 15, as storing signal patterns. Similarly, the Specification states that the output pattern memory (64) stores K number of output signal patterns.

In contrast, Okayasu does not teach either an input or output pattern memory. Applicants respectfully disagree with the Examiner that pattern generator (201) of Okayasu is a memory as claimed in claim 12. Okayasu states (col. 1, lines 24-26) that the pattern

generator (201) outputs test pattern data. Okayasu does not teach that this test pattern data was stored, as in a memory, but instead implies it is generated by the pattern generator (201).

Therefore, it is submitted that claim 12 is patentably distinguishable over the prior art and allowance of this claim is requested.

Claims 13-15 depend from claim 12 and inherently include all of the limitations of the base claim. As discussed above, the prior art does not teach the limitations of the base claim much less the further embodiments of the dependent claims. Therefore, claims 13-15 are allowable for their dependency and their own merits. Allowance of these claims is requested.

For the foregoing reasons, reconsideration and allowance of claims 1-20 of the application as amended is solicited. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Respectfully submitted,

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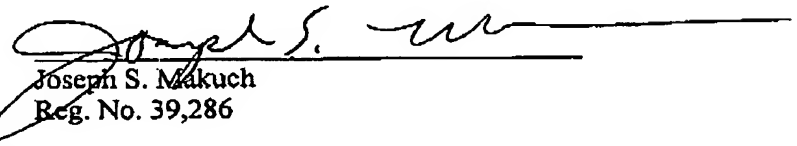

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I hereby certify that this correspondence is being transmitted to the U.S. Patent and Trademark Office via facsimile number (703) 872-9306 on June 6, 2005.

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